What is claim d is:

1. A dual damascene process for forming a multi-layer low-k interconnects, comprising the steps of:

depositing a first dielectric layer of a first low-k on a substrate;

etching said first dielectric layer for forming two dual damascene vias extending through said first dielectric layer to expose a surface of said substrate;

forming a first barrier layer for covering on said first dielectric layer and said surface;

forming two Cu conductor plugs each filled in one of said two dual damascene vias;

forming a second barrier layer for covering on said two Cu conductor plugs to enclose said two Cu conductor plugs by said first and second barrier layers;

etching-back said first dielectric layer for forming a trench between said two dual damascene vias; and

spinning-on a second dielectric layer of a second low-k smaller than said first low-k in said trench.

2. The process of claim 1, wherein said forming two Cu conductor plugs comprises the steps of:

depositing a Cu conductor layer filled in said two dual damascene vias; and

etching-back said Cu conductor layer for leaving said Cu conductor layer in said two dual damascene vias.

3. The process of claim 2, further comprising etching said first barrier layer for leaving said first barrier layer in said two dual damascene vias after said etching-back said Cu conductor layer.

4. The process of claim 1, wherein said forming a second barrier layer comprises the steps of:

depositing said second barrier layer on said two Cu conductor plugs and first dielectric layer; and

applying CMP to said second barrier layer for leaving said second barrier layer over said two dual damascene vias.

5. The process of claim 1, wherein said depositing a first dielectric layer comprises depositing a SiOC by CVD.

6. The process of claim 1, wherein said etching-back said first dielectric layer comprises wet etching said first dielectric layer.

7. The process of claim 1, further comprising etching-back said second dielectric layer for planarizing said second dielectric layer to said second dielectric layer.

8. The process of claim 7, further comprising the steps of:

depositing a third dielectric layer of a third low-k on said second dielectric and barrier layers;

etching said third dielectric and second barrier layers for forming two second dual damascene vias extending through said third dielectric and second barrier layers to expose a surface of said two Cu conductor plugs;

forming a third barrier layer for covering on said third dielectric layer and surface of said two Cu conductor plugs;

forming two second Cu conductor plugs each filled in one of said first two dual damascene vias;

forming a fourth barrier layer for covering on said two second Cu conductor plugs to enclose said two second Cu conductor plugs by said third and fourth barrier layers;

etching-back said third dielectric layer for forming a second trench between said two second dual

damascene vias; and

spinning-on a fourth dielectric layer of a fourth low-k smaller than said third low-k in said second trench.

9. A multi-layer low-k dual damascene interconnect comprising:

a first dielectric layer of a first low-k on a substrate;

a second dielectric layer of a second low-k smaller than said first low-k spun-on said first dielectric layer;

a plurality of dual damascene vias formed in said first and second dielectric layers;

a plurality of Cu conductor plugs each filled in one of said plurality of dual damascene vias; and

a barrier layer inserted between said plurality of Cu conductor plugs and first and second dielectric layers.

10. The interconnect of claim 9, wherein said first low-k has a value between 2.5 and 3.

11. The interconnect of claim 9, wherein said first dielectric layer comprises SiOC.

12. The interconnect of claim 9, wherein said second

low-k has a value smaller than 2.5.